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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,891	04/15/2004	Marc E. Goldfarb	A5WI2646US	8986

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EXAMINER	
NGUYEN, LINH M	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/825,891	GOLDFARB ET AL.
	Examiner	Art Unit
	Linh M. Nguyen	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-30 are presented in the instant application according to the Applicants' filing on 04/14/2005.

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Objections/Minor Informalities

2. Claims 22-23 and 26 are objected to because of the following informalities:

Claim 22 should be deleted since it is very similar to claim 18 which it depends on; in addition "22" in line 1 of claim 23 should be changed to --18--.

Claim 26, line 7, change "an " to -- a reference—to be consistent with limitation in lines 8-9.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-7, 11, 15, 18 and 22-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Cho (U.S. Patent No. 6,917,229).

With respect to claims 1 and 11, Cho discloses, in Figure 1, a reference signal generator, comprising an oscillator *(inherent since clock signal Clock is generated by an oscillator)* that provides an oscillator signal [Clock]; a buffer amplifier [140] having an adjustable amplifier gain and coupled to process the oscillator signal into a reference signal [output form 140] that has a reference amplitude; and a controller [120,130] that adjusts the amplifier gain in response to the reference amplitude.

With respect to claim 2, Cho discloses, in Figure 1, that the controller is configured to initiate said amplifier gain at a predetermined amplifier gain and subsequently adjust the amplifier gain to a controlled amplifier gain.

With respect to claim 3, Cho discloses, in Figure 1, that the predetermined amplifier gain is a maximum amplifier gain and the controller is configured to subsequently reduce the amplifier gain to the controlled amplifier gain.

With respect to claims 4 and 15, Cho discloses, in Figure 1, that the controller includes a comparator [120] that stops reduction of the amplifier gain when the reference amplitude corresponds to a threshold amplitude.

With respect to claim 5, Cho discloses, in Figure 1, that the predetermined amplifier gain exceeds the controlled amplifier gain.

With respect to claim 6, Cho discloses, in Figure 1, that the controlled amplifier gain exceeds the predetermined amplifier gain.

With respect to claim 7, Cho discloses, in Figure 1, that the controller includes a counter [130] set to an initial count that maximizes an amplifier gain and coupled to provide a subsequent count of a clock signal that reduces the amplifier gain; and a comparator that terminates the subsequent count in response to a reference amplitude and a threshold amplitude.

With respect to claims 18 and 22, Cho discloses, in Figure 1, that the controller includes a clock that provides a clock signal; a counter [130] that counts the clock signal to thereby generate digital gain control signal [output from 130]; and a comparator [120] that passes the clock signal to the counter in response to a comparison of said reference signal and a threshold signal.

With respect to claim 23, Cho discloses, in Figure 1, that the controller [120, 130] is configured to initially reset the counter to thereby provide an initial version of the gain control signal that maximizes the amplifier gain; and the counter counts the clock signal to cause the gain control signal to reduce the amplifier gain.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 8, 9, 12-14, 16, 20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (U.S. Patent No. 6,917,229) in view of Ooishi (U.S. Pat. No. 6,404,258).

With respect to claims 8, 12-14 and 16, Cho discloses all of the claimed limitations as expressly recited in claims 1 and 11, except for the buffer amplifier including a plurality of current generators and each of the plurality of the current generators includes a plurality of resistors; and a plurality of switches that selectively access resistors in response to the controller to thereby adjust amplifier gain and an output switch that couples selected resistors to the reference port in response to the oscillator signal.

Ooshi discloses in Fig. 34, a buffer amplifier including a plurality of current generators [82a-f, 83a-f] and each having a plurality of resistors *(82d-f, since transistors being equivalent to resistors as shown in fig. 7B of Morimura et al. (U.S. Patent No. 6,556,935)*; and a plurality of switches [82a-b] that selectively access the resistors and an output switch [80b-c] that couples selected resistors to the reference port.

To configure the circuit of Cho with a buffer amplifier including a plurality of current generators with a plurality of resistors and a plurality of switches that selectively access the resistors as taught by Ooishi so that the delay can be set to a desired value would have been

obvious to one of ordinary skill in the art at the time of the invention since Ooishi teaches that such configuration would facilitate a delay circuit that operates with stability irrespective of the operating environment can be implemented *(see Ooishi., col. 32, lines 29-40).*

With respect to claim 20, Cho discloses all of the claimed limitations as expressly recited in claim 1 encompassing the controller including a comparator that provides a gain control signal in response to the reference signal and a threshold signal, except for the buffer amplifier including a plurality of resistors; and a plurality of switches that selectively access the resistors in response to a gain control signal.

Ooshi discloses in Fig. 34, a buffer amplifier including a plurality of resistors *(82d-f, since transistors being equivalent to resistors as shown in fig. 7B of Morimura et al. (U.S. Patent No. 6,556,935)*; and a plurality of switches [82a-b] that selectively access the resistors in response to a gain control signal [VPa, VNa].

To configure the circuit of Cho with a buffer amplifier including a plurality of resistors and a plurality of switches that selectively access the resistors as taught by Ooishi so that the delay can be set to a desired value would have been obvious to one of ordinary skill in the art at the time of the invention since Ooishi teaches that such configuration would facilitate a delay circuit that operates with stability irrespective of the operating environment can be implemented *(see Ooishi, col. 32, lines 29-40).*

With respect to claims 9 and 24, the combined teaching of Cho and Ooishi teaches that the amplifier gain is less than one.

7. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (U.S. Patent No. 6,917,229) in view of Donnelly et al. (U.S. Pat. No. 6,642,746).

With respect to claim 17, Cho discloses all of the claimed limitations as expressly recited in claim 1 and 15 except for the comparator comprising a differential pair of transistors that determines the gain control signal in response to the reference signal and the threshold signal.

Donnelly et al. discloses in Fig. 3, a phase comparator comprising a differential pair of transistors [49, 50] that determines the gain control signal in response to the reference signal [Vref] and the threshold signal [Vin2].

To configure the circuit of Cho with a comparator including comprising a differential pair of transistors that determines the gain control signal in response to the reference signal and the threshold signal as taught by Donnelly et al. for minimized phase detector error would have been obvious to one of ordinary skill in the art at the time of the invention since Donnelly et al. teaches that such configuration would accurately detects the phase/gain difference between the two inputs having different voltage swing characteristics *(see Donnelly et al., col. 1, lines 32-34).*

8. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (U.S. Patent No. 6,917,229) in view of Fiscus (U.S. Pat. No. 6,492,852).

With respect to claim 19, Cho discloses all of the claimed limitations as expressly recited in claim 1 and 18 except for clock includes at least one divider that divides the oscillator signal to thereby generate the clock signal.

Fiscus discloses, in Fig. 5, a phase locked loop/delay locked loop with a pre-divider [116] for the input clock signal.

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure a divider circuit to divide the input clock signal of Cho locked loop circuit as taught by Fiscus in order to provide the required reduced frequency of the clock signal that propagates

through the delay line circuit hence reduce power consumption since such circuit arrangement of the divider circuit for the stated purpose has been a well known practice as evidenced by the teachings of Fiscus *(see Fiscus, col. 4, lines 5-9)*.

9. Claims 10 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (U.S. Patent No. 6,917,229) in view of Lin et al. (U.S. Pub. No. 2005/0093638 A1).

With respect to claims 10 and 25, Cho discloses all of the claimed limitations as expressly recited in claim 1, except for the oscillator which generated the reference clock signal specifically being a digitally-controlled crystal oscillator.

Lin et al. discloses, in Fig. 2 and paragraph [0007], a digitally-controlled crystal oscillator and its advantages.

To configure the circuit of Cho with a digitally-controlled crystal oscillator as taught by Lin et al. to control more precisely the resonant frequency of the crystal oscillator by including a processing portion that monitors the resonant frequency produced by a crystal oscillator and alters the resonant frequency of the crystal oscillator by changing the capacitive loading on the crystal oscillator to tune the frequency of the crystal oscillator would have been obvious to one of ordinary skill in the art at the time of the invention since such circuit arrangement of the digitally-controlled crystal oscillator for the stated purpose has been a well known practice as evidenced by the teachings of Lin et al. *(see Lin et al., paragraph [0007], lines 4-13)*.

10. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (U.S. Patent No. 6,917,229) in view of Ooishi (U.S. Pat. No. 6,404,258), as applied in claim 20, and further in view of Donnelly et al. (U.S. Patent No. 6,642,746).

The combined teaching of Cho and Ooishi discloses all the claimed limitations as expressly recited in claim 20 except for the comparator comprising a differential pair of transistors that determines the gain control signal in response to the reference signal and the threshold signal.

Donnelly et al. discloses in Fig. 3, a phase comparator comprising a differential pair of transistors [49, 50] that determines the gain control signal in response to the reference signal [Vref] and the threshold signal [Vin2].

To configure the combined circuit of Cho and Ooishi with a comparator including comprising a differential pair of transistors that determines the gain control signal in response to the reference signal and the threshold signal as taught by Donnelly et al. for minimized phase detector error would have been obvious to one of ordinary skill in the art at the time of the invention since Donnelly et al. teaches that such configuration would accurately detects the phase/gain difference between the two inputs having different voltage swing characteristics *(see Donnelly et al., col. 1, lines 32-34).*

11. Claims 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (U.S. Patent No. 6,917,229) in view of Fiscus (U.S. Patent No. 6,492,852) and in view of Li (U.S. Pub. No. 2005/0046495).

With respect to claim 26, Cho discloses a synthesizer comprising a buffer amplifier [110] having an adjustable amplifier gain and coupled to process an oscillator signal [Clock, generated from an oscillator] into a reference signal that has a reference amplitude; and a controller [120, 130] that adjusts the amplifier gain in response to the reference amplitude.

Cho fails to disclose a first frequency divider, a second frequency divider, a voltage-controlled oscillator and a phase detector that provides a control signal to the voltage-controlled oscillator;

Fiscus discloses, in Fig. 5, a locked loop comprising a first frequency divider [116]; a second frequency divider.

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure a divider circuit to divide the input clock signal of Cho locked loop circuit as taught by Fiscus in order to provide the required reduced frequency of the clock signal that propagates through the delay line circuit hence reduce power consumption,since such circuit arrangement of the divider circuit for the stated purpose has been a well known practice as evidenced by the teachings of Fiscus *(see Fiscus, col. 4, lines 5-9)*.

The combined teaching of Cho and Fiscus fails to disclose fails to disclose a voltage-controlled oscillator and a phase detector that provides a control signal to the voltage-controlled oscillator.

Li discloses, in Figs. 6-7, a circuit encompassing two locked loop circuits [Fig. 6] and the details of one of the locked loop circuits [Fig.7] with a voltage-controlled oscillator [300] and a phase detector [700] that provides a control signal to the voltage-controlled oscillator.

To configure the circuit of the combined teaching of Cho and Fiscus in the same arrangement as shown in Fig. 6 and with a voltage-controlled oscillator and a phase detector [Fig. 7] as taught by Li for phase noise cleaning up would have been obvious to one of ordinary skill in the art at the time of the invention since Li teaches that such configuration would

minimize the phase noise thus improve the circuit performance *(see Li, paragraph [0034] col. 1, lines 32-34).*

With respect to claim 27, the combined teaching of Cho, Fiscus and Li discloses that the controller [120, 130] is configured to initiate the amplifier gain at a maximum amplifier gain; and subsequently reduce the amplifier gain to a controlled amplifier gain.

With respect to claim 28, the combined teaching of Cho, Fiscus and Li discloses that the controller includes a comparator [120] that stops reduction of the amplifier gain when the reference amplitude corresponds to a threshold amplitude.

With respect to claim 29, the combined teaching of Cho, Fiscus and Li discloses that the controller [120, 130] includes a clock that provides a clock signal; a counter set to an initial count that maximizes the amplifier gain and coupled to provide a subsequent count of the clock signal that reduces the amplifier gain; and a comparator that terminates said subsequent count in response to the reference amplitude and a threshold amplitude.

12. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (U.S. Patent No. 6,917,229) in view of Fiscus (U.S. Patent No. 6,492,852) and in view of Li (U.S. Pub. No. 2005/046495), as applied in claim 26, and further in view of Ooishi (U.S. Pat. No. 6,404,258).

With respect to claim 30, the combined teaching of Cho, Fiscus and Li discloses all of the claimed limitations as expressly recited in claim 26, except for the buffer amplifier including a plurality of resistors; and a plurality of switches that selectively access the resistors in response to the controller to thereby adjust amplifier gain.

Ooshi discloses in Fig. 34, a buffer amplifier including a plurality of current generators [82a-f, 83a-f] and each having a plurality of resistors *(82d-f, since transistors being equivalent to*

resistors as shown in fig. 7B of Morimura et al. (U.S. Patent No. 6,556,935); and a plurality of switches [82a-b] that selectively access the resistors and an output switch [80b-c] that couples selected resistors to the reference port.

To configure the circuit of the combined teaching of Cho, Fiscus and Li with a buffer amplifier including a plurality of current generators with a plurality of resistors and a plurality of switches that selectively access the resistors as taught by Ooishi so that the delay can be set to a desired value would have been obvious to one of ordinary skill in the art at the time of the invention since Ooishi teaches that such configuration would facilitate a delay circuit that operates with stability irrespective of the operating environment can be implemented *(see Ooishi., col. 32, lines 29-40)*.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

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PRIMARY EXAMINER